

# Balanced Linear-Phase Bandpass Filter Equalized with Negative Group Delay Circuit

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**Abstract.** A novel balanced linear-phase bandpass filter is proposed to achieve differential-mode linear-phase filtering and common-mode suppression characteristics. The balanced linear-phase bandpass filter consists of a proposed compact balanced bandpass filter and negative group delay circuits, in which the circuits are loaded on the ports of the filter as branches. The linear-phase performance is achieved through negative compensation of group delay fluctuations using negative group delay circuit equalization. In order to verify the design method, a 3-order balanced linear-phase bandpass filter is designed, simulated, manufactured, and measured. The results show that the group delay fluctuation of the balanced bandpass filter has been reduced by 89.6% from 1.110 to 0.115 ns. The minimum common-mode suppression within the passband is 41.4 dB. The proposed balanced bandpass filter has an excellent differential-mode linear-phase transmission and common-mode suppression performances.

## Keywords

Balanced bandpass filter, linear-phase, negative group delay, common-mode suppression

## 1. Introduction

Balanced bandpass filters (BPF) are widely applied in balanced circuits and systems to suppress common-mode (CM) noise and electromagnetic interference [1–3]. In communication systems, BPF often causes group delay (GD) fluctuations within the passband, and the fluctuations become severe accompanied by the improvement of BPF frequency selection performance, leading to an increase in system bit error rate and a decrease in communication quality [4]. To ensure the undistorted transmission of passband signals, linear-phase BPF can be used to achieve flat phase-frequency response [5].

Linear-phase BPF can be realized by substrate integrated waveguide [5], [6], high-temperature superconduct-

ing (HTSC) [7–10], microstrip circuit (MC) [11–13], etc. Compared to other methods, microstrip circuits have been extensively applied due to the advantages of low cost, lightweight, simple production and convenient integration. In the application of the microstrip circuits, the research of the negative group delay (NGD) technology provides a solution for improving the GD performance [14–16]. Therefore, the negative group delay circuit (NGDC) could be applied as an equalizer to BPF to reduce GD fluctuations and achieve linear-phase characteristics.

Generally, linear-phase BPF mainly implemented through self-equalization and external-equalization method, achieving phase flatness performance [11–13]. The self-equalization linear-phase BPF proposed in [11] and [12] utilized NGD compensated admittance inverter (J-inverter) to displace the J-inverter of BPF with half-/quarter-wavelength shunt stubs and achieve linear-phase characteristics. Both of the NGD compensated J-inverters consist of coupled lines, short- or open-circuited lines, and resistors. The NGD frequency and GD value can be regulated by setting the electrical parameters of microstrip lines and resistance value of resistors, respectively. However, the self-equalization linear-phase BPF proposed in [11] and [12] were designed based on the BPF with half-/quarter-wavelength shunt stubs, owing to the inherent characteristic of the shunt stub resonators, parasitic passband presence at the second harmonic of the center frequency, which deteriorates the frequency selection characteristic of BPF. Correspondingly, the external equalization method compensates for GD by loading NGDC on the input/output ports of the BPF circuit instead of changing the BPF structure to achieve the linear-phase characteristics [13]. However, ports impedance mismatch was occurred while loading NGDC. Thus, the linear-phase BPF proposed in [13] adopted two pairs of Wilkinson power dividers and asymmetric configuration of NGDCs to achieve input/output port impedance matching, which increased significantly the circuit size.

So far, all researches on linear-phase BPF were unbalanced circuits. To the best of the author's knowledge, previous reports have not discovered the design of bal-

anced linear-phase BPF yet. Considering the wide application of balanced circuits, it is necessary to propose a balanced linear-phase BPF.

In this paper, a balanced BPF is proposed based on stepped impedance resonators (SIR) and stub-loaded ring resonator (SLRR), which has excellent differential-mode (DM) transmission and common-mode suppression (CMS). Furthermore, linear-phase performance is achieved by equalizing with the NGDC. For demonstration, the proposed balanced BPF and the balanced linear-phase BPF are designed and manufactured. It shows high consistency between the simulation and measured results, which verifies the proposed design method.

## 2. Circuit Structure and Theoretical Analysis

### 2.1 Design Theory of the Proposed Balanced BPF

The equivalent circuit of the proposed balanced BPF is depicted in Fig. 1, where the circuit consists of double balanced ports (ports A+ and A-, ports B+ and B-),  $C_m$ ,  $L_m$ , and  $C_{gn}$  ( $n = 1, 2$ ) are equivalent lumped components of the resonant units (capacitors  $C_{rn}$  and inductors  $L_{rn}$  determine the center frequency of the BPF,  $C_{gn}$  is indispensable for DM transmission of the balanced BPF and influence the CMS characteristic), and  $J_{m,m+1}$  ( $m = 0, 1, 2, 3$ ) are J-inverters which are coupling the resonators [17]. Under the DM and CM excitation, the central horizontal plane corresponds to the electric and magnetic wall, and the equivalent unit respectively corresponds to the bandpass (\* in Fig. 1 represented  $L_{rn}$  are grounded when DM excitation) and stopband functional units, which is overall corresponds to DM transmission and CMS. Implementing the physical microstrip circuit based on the equivalent circuit, where the LC lumped components are materialized as SIR and SLRR which are depicted in Figs. 2(a) and 2(b), while the J-inverters are implemented as the magnetic coupling between resonators.

The input admittance of the resonators can be expressed as

$$Y_{in1} = \frac{Z_1 - Z_2 \tan \theta_1 \tan \theta_2}{jZ_1^2 \tan \theta_1 + jZ_1 Z_2 \tan \theta_2}, \quad (1)$$

$$Y_{in2} = \frac{2X_0 - 2Z_3 X_5 \tan \theta_4 - Z_4 \tan \theta_3 (X_4 + X_5)}{j(X_0 X_5 + X_0 X_4 + 2X_3 Z_4 - 2 \tan \theta_4 X_3 X_5)} \quad (2)$$

where  $X_0 = Z_3 Z_4$ ,  $X_1 = Z_4 Z_5$ ,  $X_2 = Z_3 Z_5$ ,  $X_3 = Z_3 \tan \theta_3$ ,  $X_4 = Z_4 \tan \theta_4$  and  $X_5 = Z_5 \tan \theta_5$ .

According to the resonance condition  $Y_{in} = 0$ , meanwhile, in this design,  $Z_2 = Z_5$ , and  $\theta_2 = \theta_5$ . Thus the resonance conditions of the resonators are denoted by

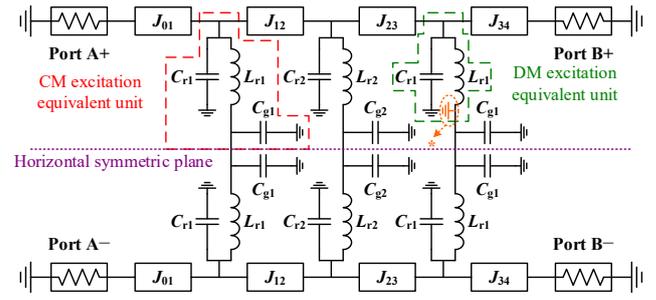


Fig. 1. Equivalent circuit of the proposed balanced BPF.

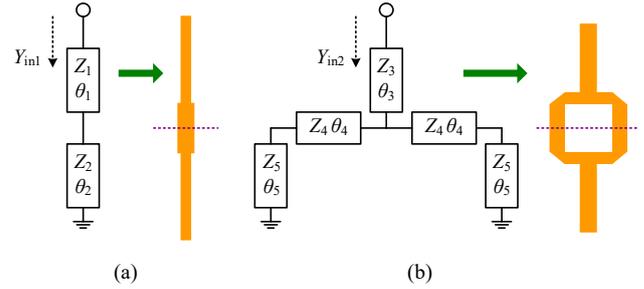


Fig. 2. Schematic (under DM excitation) and layout of the resonators. (a) SIR, (b) SLRR.

$$\frac{Z_1}{\tan \theta_1} = Z_2 \tan \theta_2, \quad (3)$$

$$\frac{Z_3}{\tan \theta_3} = \frac{X_5 Z_4 + Z_4^2 \tan \theta_4}{2Z_4 - 2X_5 \tan \theta_4}. \quad (4)$$

According to (3),  $Z_1(W_1)$ ,  $\theta_1(L_1)$ ,  $Z_2(W_3)$ , and  $\theta_2(L_3/2)$  determine the resonant response of the SIR. For the SLRR, it is generally utilized as a dual-mode resonator in BPF to realize the wide-band or dual-band characteristics [18], [19]. In this design, it is employed as a single-mode resonator by adjusting the electrical parameters of the transmission lines in the SLRR based on (4) to reduce filter size. And  $Z_4(W_4)$ ,  $\theta_4(L_4)$  can be set firstly to simplify the design, and finally, the resonant response of the SLRR can be determined by  $Z_3(W_2)$  and  $\theta_3(L_2)$ .

The proposed balanced BPF is composed of triple resonators (double SIR resonators and a SLRR resonator)

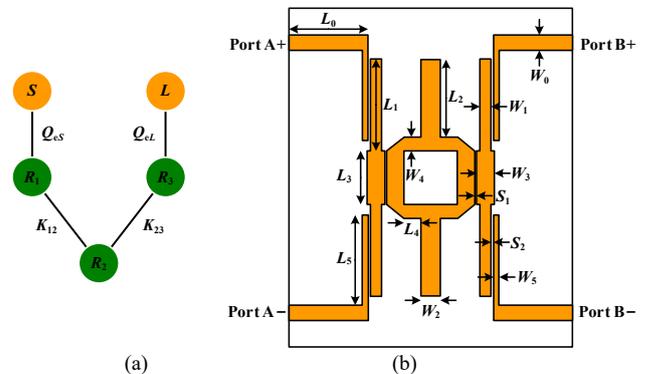


Fig. 3. (a) Equivalent coupling routing scheme of the proposed balanced BPF. (b) Layout of the proposed balanced BPF.

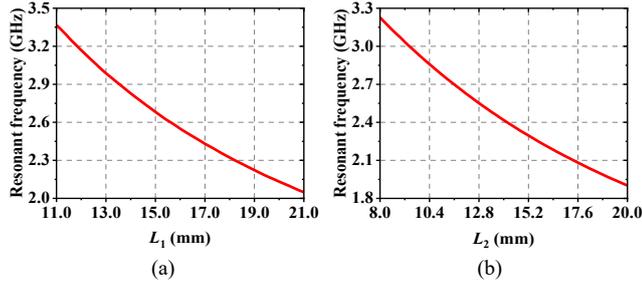


Fig. 4. Relation curves between physical size and resonant frequency of resonators: (a)  $L_1$ , (b)  $L_2$ .

through magnetic coupling, as shown in Fig. 3. Correspondingly, the layout of the proposed balanced BPF microstrip circuit is shown in Fig. 3(b). The frequency responses of SIR and SLRR are determined by their physical dimensions, which are respectively illustrated in Figs. 4(a) and 4(b) with varied  $L_1$  and  $L_2$  (where  $W_1 = 2.0$  mm,  $W_2 = 3.4$  mm,  $L_3 = 9.5$  mm,  $W_3 = 3.1$  mm,  $L_4 = 3.0$  mm, and  $W_4 = 2.5$  mm).

The center frequency of the proposed balanced BPF passband is specified at 2.45 GHz. For DM excitation, the symmetry plane of the resonator is the electrical wall (short-circuited). The DM excitation first-mode resonant frequency  $f_{r1}$  of SIR and SLRR should coincide at the specified frequency. Meanwhile, the second-mode resonant frequency  $f_{r2}$  of SIR and SLRR should be misaligned in order to eliminate DM parasitic passband. For CM excitation, the symmetry plane is the magnetic wall (open-circuited), and the CM excitation resonant frequency  $f_{r1}'$  and  $f_{r2}'$  of SIR and SLRR should be away from the desired passband to achieve the CMS performance. In the case of weak coupling, the insertion loss (IL) of the two resonators which are excited under DM and CM excitation are simulated and shown in Figs. 5(a) and 5(b), respectively.

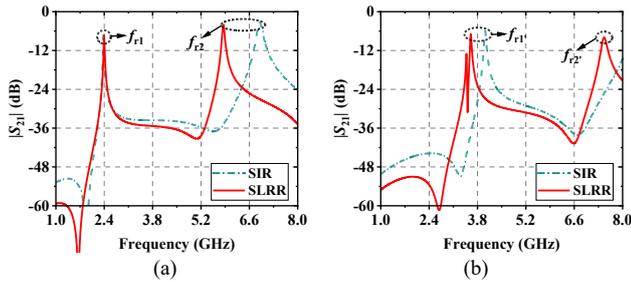


Fig. 5. Simulated IL under the weak coupling of the resonators: (a) DM excitation, (b) CM excitation.

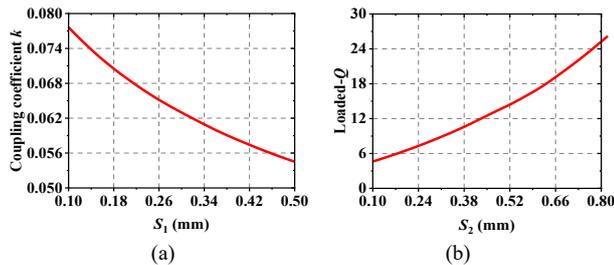


Fig. 6. Relation curves between physical size and parameters of the BPF: (a) coupling coefficient  $k$ , (b) loaded- $Q$ .

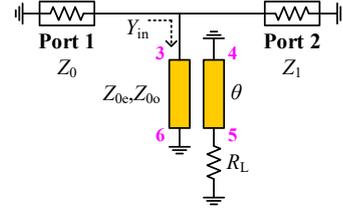


Fig. 7. Schematic of the NGDC branch.

To investigate the effects of the coupling coefficient and loaded quality factor (loaded- $Q$ ,  $Q_{eS}$  and  $Q_{eL}$ ), presuming the bandwidth and return loss (RL) of the proposed balanced BPF are 230 MHz and 22 dB, the key parameters  $S_1$  and  $S_2$  are tuned in Figs. 6(a) and 6(b) to satisfy the design performance.

## 2.2 NGDC Analysis

The balanced linear-phase BPF mainly achieves GD flatness characteristics by NGDC equalizing branches, which schematic diagram of NGDC is depicted in Fig. 7. The NGDC consists of two-terminal short-circuited coupled lines (TSCL) and a grounding resistor. In [14], the NGDC branch is a reflection-type circuit, where an extra  $90^\circ$  hybrid coupler is needed to convert the circuit to transmission-type and realize port matching [14]. In this design, the NGDC circuit is used as a parallel branch, the input admittance  $Y_{in}$  of which is about 0, so it doesn't affect the port matching and can be used to equalize the group delay of the proposed balanced BPF.

For the TSCL section, the electrical length  $\theta$  is  $\pi/2$  at the NGDC center frequency of  $f_n$ , the even- and odd-mode characteristic admittances are expressed as  $Y_{0e}$  and  $Y_{0o}$ , respectively. The resistance value of the grounding resistor is represented as  $R_L$ . The TSCL's terminal port 5 connects the grounding resistor  $R_L$ , terminal ports 4 and 6 are short-circuited, and the terminal port 3 connects to the proposed balanced BPF circuit. The input impedance  $Y_{in}$  at the TSCL's terminal port 3 with grounding resistor terminated at the terminal port 5 and the admittance matrix of the TSCL [20] are obtained as (5) and (6), respectively:

$$Y_{in} = Y_{33} - \frac{Y_{35}Y_{53}}{Y_{55} + G_L}, \quad (5)$$

$$\begin{bmatrix} Y_{33} & Y_{35} \\ Y_{53} & Y_{55} \end{bmatrix} = \begin{bmatrix} -j \frac{Y_{0o} + Y_{0e}}{2} \cot \frac{\pi f}{2f_n} & -j \frac{Y_{0o} - Y_{0e}}{2} \csc \frac{\pi f}{2f_n} \\ -j \frac{Y_{0o} - Y_{0e}}{2} \csc \frac{\pi f}{2f_n} & -j \frac{Y_{0o} + Y_{0e}}{2} \cot \frac{\pi f}{2f_n} \end{bmatrix}. \quad (6)$$

Therefore, the input admittance  $Y_{in}$  is calculated as

$$Y_{in} = \frac{A^2 - j2AG_L - B^2}{j2A + 4G_L} \quad (7)$$

where

$$A = (Y_{0o} + Y_{0e}) \cot \frac{\pi f}{2f_n}, B = (Y_{0o} - Y_{0e}) \csc \frac{\pi f}{2f_n}. \quad (8)$$

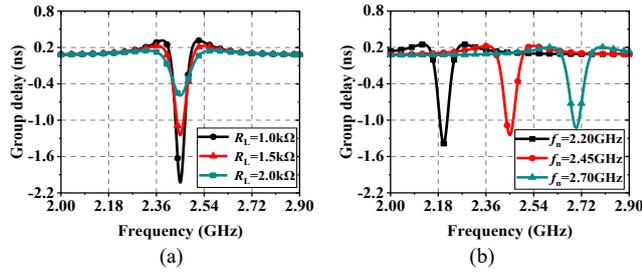


Fig. 8. The GD responses of the NGDC with different parameters: (a)  $R_L$ , (b)  $f_n$ .

In Fig. 7, the port impedance of ports 1 and 2 are  $Z_0$  and  $Z_1$ , respectively, thus the  $S_{21}$  can be obtained as

$$S_{21} = \frac{2}{1 + Y_{in}Z_0 + Z_0/Z_1}. \quad (9)$$

The group delay is expressed as

$$\tau = -\frac{1}{2\pi} \frac{d\angle S_{21}(f)}{df}. \quad (10)$$

According to the above theoretical derivation, the ideal microstrip lines and lumped component are adopted for analysis, and the results are shown in Fig. 8. From Fig. 8(a), it can be observed that the NGD value can be adjusted by tuning the value of  $R_L$  and the center frequency of NGD can be changed by tuning the  $f_n$  from Fig. 8(b) (Assuming  $Z_c = 45 \Omega$ ,  $Z_o = 34 \Omega$ ,  $Z_0 = Z_1 = 50 \Omega$ ).

### 2.3 Design Procedure

Based on the circuit analysis theory mentioned above, the design process of the proposed balanced linear-phase BPF equalized with NGDC in this paper is summarized as follows:

*Step 1:* Determine the filtering performance of the proposed balanced BPF. Calculate the dimensions of the SIR and SLRR resonators besides verifying the first- and high-mode resonant frequencies under DM and CM excitation to ensure DM transmission and CMS.

*Step 2:* Calculate and adjust the coupling coefficient and loaded- $Q$  according to the filter design theory corresponding to the key parameters  $S_1$  and  $S_2$ , and finally obtain the required BPF by optimizing the parameters.

*Step 3:* On the basis of the group delay characteristics of the BPF designed in *Step 2*, determine the required GD fluctuation compensate performance, the electrical parameters of the NGDC are designed based on the frequency, bandwidth, and group delay amplitude of the required NGDC equalization.

*Step 4:* Equalized with the NGDC of the proposed balanced BPF, which is shown in Fig. 9, performing simulation and parameter adjustment on the NGDC Unit 1 and 2 (The NGDC units in the upper part of the circuit are the same as those marked in the lower parts, and are symmetrical about the horizontal central symmetry plane), and obtain the final layout dimensions of the proposed balanced linear-phase BPF.

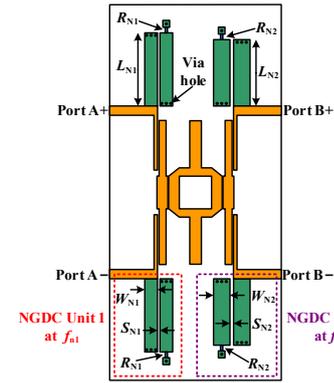


Fig. 9. Schematic of the proposed balanced linear-phase BPF.

## 3. Simulation and Experimental Verification

The proposed balanced BPF adopts the design method of Chebyshev response filter. Applying the above-mentioned balanced linear-phase BPF design theory, a 3-order balanced linear-phase BPF is designed, with the passband center frequency  $f_0$  of 2.45 GHz, the bandwidth of 230 MHz and the RL is 22 dB. The circuit adopts F4B high-frequency substrate board (circuit size:  $50 \times 60 \times 1 \text{ mm}^3$ ), with a relative dielectric constant of 2.6 and a loss tangent of 0.003. According to microwave engineering and Chebyshev theory, the required ripple coefficient can be obtained as 0.027 dB, and the normalized component values can be obtained as  $g_0 = 1$ ,  $g_1 = 1.261$ ,  $g_2 = 1.7459$ ,  $g_3 = 1.261$  and  $g_4 = 1$ . Considering the center frequency  $f_0$  and bandwidth, obtain the coupling coefficients  $K_{01} = 0.083599$ ,  $K_{12} = 0.063269$ ,  $K_{23} = 0.063269$ ,  $K_{34} = 0.083599$ , and  $Q_{eS} = Q_{eL} = 13.433$ . Applying Ansys HFSS® software, simulating, optimizing and determining the final physical dimensions of the proposed balanced BPF are shown in Tab. 1.

$L_0$	$W_0$	$L_1$	$W_1$	$L_2$	$W_2$	$S_1$
13.9	2.72	16.35	2.00	13.72	3.40	0.28
$L_3$	$W_3$	$L_4$	$W_4$	$L_5$	$W_5$	$S_2$
9.50	3.10	3.00	2.50	16.00	1.00	0.445

Tab. 1. The optimized physical dimensions of the proposed balanced BPF (unit: mm).

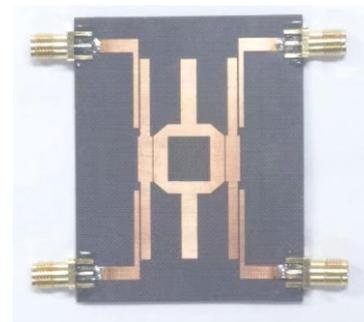


Fig. 10. Photograph of the proposed balanced BPF.

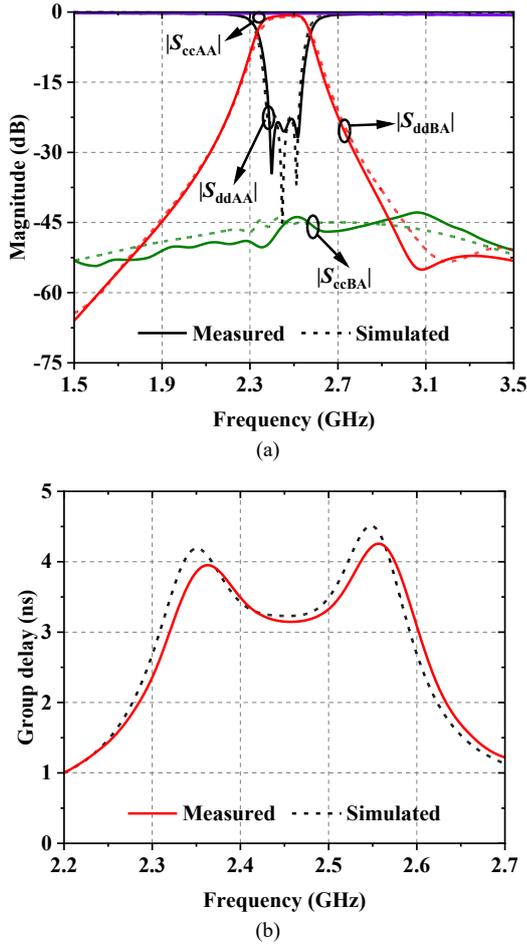


Fig. 11. Measured results of the proposed balanced BPF. (a) Mixed  $S$ -parameters. (b) GD within the passband.

Figure 10 shows the photograph of the proposed balanced BPF, while Figures 11(a) and 11(b) show the mixed  $S$ -parameters and GD measured results of the proposed balanced BPF. According to Fig. 11(a), the measured DM minimum IL within the passband is 0.98 dB, the DM 3-dB passband bandwidth is 225 MHz (2.349–2.574 GHz), the DM 10-dB RL bandwidth is 2.362–2.553 GHz, and the minimum CMS is 43.83 dB, meeting the design requirements. According to Fig. 11(b), the GD fluctuation within the passband is 1.11 ns and the measured GD fluctuation extremum are around 2.363 GHz and 2.557 GHz while the simulated GD fluctuation extremum are around 2.35 GHz and 2.548 GHz.

Set  $f_{n1} = 2.35$  GHz and  $f_{n2} = 2.548$  GHz, after calculation and optimization, the electrical parameters and physical dimensions of the NGDCs are shown in Tab. 2, in which  $Z_{0e-Nx}$  and  $Z_{0o-Nx}$  ( $x = 1, 2$ ) represent the electrical pa-

$Z_{0e-N1}$	$Z_{0o-N1}$	$Z_{0e-N2}$	$Z_{0o-N2}$	$R_{N1}$	$R_{N2}$
45.34 $\Omega$	34.47 $\Omega$	36.55 $\Omega$	30.15 $\Omega$	768.00 $\Omega$	1.58 k $\Omega$
$L_{N1}$	$W_{N1}$	$S_{N1}$	$L_{N2}$	$W_{N2}$	$S_{N2}$
21.48 mm	3.70 mm	0.70 mm	19.45 mm	4.80 mm	1.00 mm

Tab. 2. The optimized electrical parameters and physical dimensions of the NGDCs.

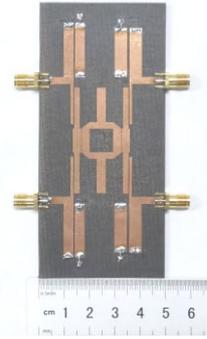


Fig. 12. Photograph of the proposed balanced linear-phase BPF.

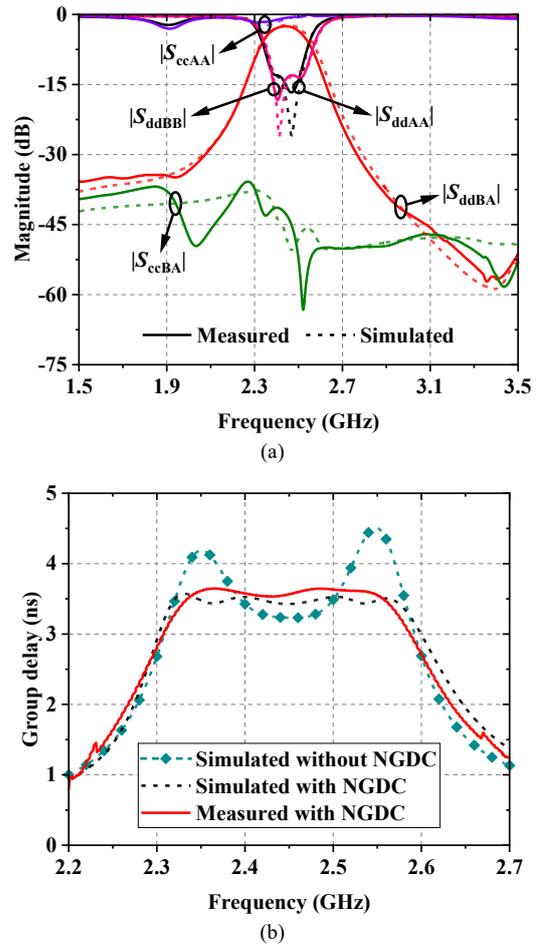


Fig. 13. Measured results of the balanced linear-phase BPF. (a) Mixed  $S$ -parameters. (b) GD.

rameters of the NGDC Unit 1 and 2, corresponding to physical dimensions  $L_{Nx}$ ,  $W_{Nx}$ , and  $S_{Nx}$ . The resistors are packaged in 0806 (commercial products with 1% accuracy), the grounding terminals of the grounding resistors have solder pads size of  $2.0 \times 2.0$  mm<sup>2</sup>, and the grounding via holes of the coupled lines as well as grounding terminals with a diameter of 0.5 mm. Figure 12 shows the photograph of the proposed balanced linear-phase BPF (circuit size:  $50 \times 110 \times 1$  mm<sup>3</sup>).

Figure 13 shows the measured results of the proposed balanced linear-phase BPF, where  $|S_{ddBA}|$  and  $|S_{ccBA}|$  are the

Refs.	$f_0$ (GHz)	3-dB BW (%)	GD Fluctuation Reduction (ns)	GD Fluctuation (ns)	$\Delta_{FGD}$ (%)	IL (dB)	Implement Method	Balanced Circuit	CMS
[7]	2.25	0.62	-	10	59.7	2.09	HTSC	No	-
[8]	0.254	2.76	-	50	50	0.24	HTSC	No	-
[9]	8.63	0.49	-	23	78.5	1.60	HTSC	No	-
[10]	2.00	1.5	-	10	60	0.30	HTSC	No	-
[11]	2.45	25	0.19	0.21	100	0.53	Microstrip	No	-
[12]	2.00	50	0.41	0.18	124.5	-	Microstrip	No	-
[13]	2.45	27	0.42	0.15	100	2.14	Microstrip	No	-
This work	2.44	8.03	0.995	0.115	110.7	2.54	Microstrip	Yes	41.4

**Tab. 3.** Performance comparisons between the proposed balanced linear-phase BPF and previous linear-phase BPFs.

differential- and common-mode transmission coefficients from the balanced port A to B, respectively.  $|S_{ddAA}|$  is the DM reflection coefficient at the balanced port A.  $|S_{ccAA}|$  is the CM reflection coefficient at the balanced port A. The results show that the IL for DM transmission is 2.54 dB, the DM 3-dB passband bandwidth is 196 MHz (2.342–2.538 GHz), the DM 10-dB RL bandwidth for port A and port B are 2.360–2.524 GHz and 2.365–2.547 GHz, respectively. The minimum CMS is 41.4 dB. The GD fluctuation within the passband is less than 0.115 ns, reduced by 89.6% (0.995 ns).

Table 3 compares the results of the proposed design with previous linear-phase BPF results. Linear-phase BPFs published in [7–10] are implemented based on HTSC method, but the implementation of the HTSC is difficult and the production cost is expensive. Linear-phase BPFs published in [11–13] and the method proposed in this paper are implemented based on microstrip circuits which are simple to achieve and the cost is low-priced. The results show that compared to the linear-phase BPFs published in other papers, the GD fluctuation reduction of the proposed method is 0.995 ns which is greater than other linear-phase BPFs, and the GD fluctuation of 0.115 ns is more smooth than those in other papers to ensure the flatness of GD. It should be noted that the proposed linear-phase filter in this paper has the smallest GD fluctuation compared to other filters. To achieve full passband linear-phase characteristic and minimize GD fluctuation, a larger absolute value of NGD is required, resulting in a larger IL. Except [12], the flat group delay (FGD) bandwidth ratio  $\Delta_{FGD}$  of 110.7 % is better than other published papers.  $\Delta_{FGD}$  is defined as

$$\Delta_{FGD} = \frac{BW_{FGD}}{BW_{3-dB}} \quad (11)$$

where  $BW_{FGD}$  represents the flat group delay bandwidth,  $BW_{3-dB}$  represents the DM 3-dB passband bandwidth of the linear-phase BPF.

## 4. Conclusions

The first design of the balanced linear-phase bandpass filter has been presented in this paper. The design theory of the proposed balanced linear-phase BPF has investigated, and microstrip prototypes have been simulated, fabricated and measured to demonstrate the design principle. High performance of balanced linear-phase bandpass filtering has been achieved by designing a flexible and compact filtering structure and loading NGDCs at the input/output ports. Besides, the excellent common-mode suppression has been obtained. The proposed balanced linear-phase BPF is anticipated to improve the performance of the electronic and communication systems.

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